Op. Code	Mnem-onic	Format	Type	L/S bit	Cond. Reg.	Re-marks	Execution time μsec P855	P860	Page
1000	WIM	0	I/O	-	(3)	(k)	2.6	2.28	3
1000	WM2	0	I/O	-	(3)	(k)		2.28	4
1001	RCA	0	I/O	-	(3)	(k)	3.6	2.52	4
0101	ENB	0	M	-	(3)	(c)	1.9	1.56	1
0100	HLT	0	M	-	(3)	(k)	1.9	1.56	1
0100	RIT	0	M	-	(3)	(k)	1.9	1.56	1
0100	INH	0	M	-	(3)	(k)	1.9	1.56	1
0101	LKM	0	M	-	(3)	(c)	1.9	1.56	2
0101	SMD	0	M	-	(3)	(c)	1.9	1.56	2

KEY

Condition register

(1) CR = 0 if result = 0
1 if result > 0
2 if result < 0

(2) CR = 0 if result = 0
1 if result > 0
2 if result < 0
3 if overflow

(3) CR = Unchanged

(4) CR = 0 if a = b
1 if a > b
2 if a < b

(5) CR = 0 if command accepted
1 if command not accepted
3 if device address unknown

Remarks

(a) if R1 = 1111: System mode
if T3B type: System mode

(b) if L/S = 1: R1 ≠ 0

(c) use not restricted

(d) 'Stack overflow' when pointer has reached word address 128_{10}.

(e) R1 ≠ 0

(f) if L/S = 0: R1 ≠ 0

(g) R2 ≠ 0

(h) If R2 = 1111: System mode

(i) R3 ≠ 0

(k) restricted to system mode

(l) device address ≠ 0

Type

MR Memory Reference
RR Register/Register
K Constant
S Shift
I/O Input/Output
M Miscellaneous

Summary of P855/P860 Instruction Set

Op. Code	Mnem-onic	Format	Type	L/S bit	Cond. Reg.	Re-marks	Execution time μsec P855	P860	Page
0000	LD	1	MR	0	(1)	(a)	3.6	2.52	1
0000	ST	1	MR	1	(3)	(a)	4.8	3.36	1
0010	AD	1	MR	0/1	(2)	(a) (b)	3.6	2.52	1
0011	SU	1	MR	0/1	(2)	(a) (b)	3.6	2.52	2
0100	AN	1	MR	0/1	(1)	(a)	3.6	2.52	2
0101	OR	1	MR	0/1	(1)	(a)	3.6	2.52	3
0110	XR	1	MR	0/1	(1)	(a)	3.6	2.52	3
0010	IM	1	MR	1	(2)	(c)	4.8	3.36	4
0011	C2	1	MR	1	(2)	(c)	4.8	3.36	4
0111	ML	1	MR	0	(1)	(a)	(n+1).1.2;	(n+1).0.84	4
0111	MS	1	MR	1	(3)	(a)	N.1.9+1.2;	N.1.56+0.84	4
0001	ABI	1	MR	0	(3)	(c)	1.9	1.56	5
1110	CFI	1	MR	1	(3)	(a) (d)	5.76	4.68	5
1111	CI	1	MR	0/1	(1)	(a)	3.6	2.52	6
1101	CW	1	MR	0	(4)	(a)	3.6	2.52	6
1101	CC	1	MR	1	(4)	(a)	3.6	2.52	6
1100	LC	1	MR	0	(3)	(a) (e)	3.6	2.52	7
1100	SC	1	MR	1	(3)	(a) (e)	4.8	3.36	7
1010	RF	0	MR	n.s.	(3)	(c)	1.9	1.56	10
1011	RB	0	MR	n.s.	(3)	(c)	1.9	1.56	10
1000	MU	1	MR	0	(2)	(c)	8.04	7.68	9
1001	DV	1	MR	0	(2)	(c)	9.48	9.12	9
1010	DA	1	MR	0	(2)	(c)	3.4	3.0	8
1011	DS	1	MR	0	(2)	(c)	3.4	3.0	8
0000	LDR	1	RR	0/1	(1)	(a)	1.9	1.56	1
0000	STR	1	RR	1	(3)	(a) (d)	1.9	1.56	1
0010	ADR	1	RR	0/1	(2)	(a) (b)	1.9	1.56	1
0011	SUR	1	RR	0/1	(2)	(a) (b)	1.9	1.56	2
0100	ANR	1	RR	0/1	(1)	(a)	1.9	1.56	2
0101	ORR	1	RR	0/1	(1)	(a)	1.9	1.56	3
0110	XRR	1	RR	0/1	(1)	(a)	1.9	1.56	3

Op. Code	Mnemonic	Format	Type	L/S bit	Cond. Reg.	Remarks	Execution time μsec P855	P860	Page
0010	IMR	1	RR	1	(2)	(c)	1.9	1.56	4
0011	C2R	1	RR	1	(2)	(c)	1.9	1.56	4
0111	MLR	1	RR	0	(1)	(a)	(n+1).1.2	(n+1).0.84	4
0111	MSR	1	RR	1	(3)	(a) (d)	N.1.9+1.2	N.1.56+0.84	5
0001	ABR	1	RR	0/1	(3)	(c)	1.9	1.56	5
1110	CFR	1	RR	1	(3)	(a) (d)	1.9	1.56	6
1111	C1R	1	RR	0/1	(1)	(a) (f)	1.9	1.56	6
1101	CWR	1	RR	0/1	(4)	(a)	1.9	1.56	7
1101	CCR	1	RR	1	(4)	(a)	1.9	1.56	7
1100	LCR	1	RR	0	(3)	(a)	1.9	1.56	7
1100	SCR	1	RR	1	(3)	(a)	1.9	1.56	7
1110	RTN	1	RR	0	PSW(6-7)→CR	(g) (h)	4.3	3.24	8
1100	ECR	1	RR	n.s.	(3)	(a)	1.9	1.56	8
1000	MUR	1	RR	0	(2)	(c)	8.04	7.68	8
1001	DVR	1	RR	0	(2)	(c)	9.48	9.12	9
1010	DAR	1	RR	0	(2)	(c)	3.4	3.0	9
1011	DSR	1	RR	0	(2)	(c)	3.4	3.0	9
0100	TM	1	RR	1	(1)	(a)	1.92	1.56	9
0110	TNM	1	RR	1	(1)	(a)	1.92	1.56	10
0000	LDK	0/1	K	-/0	(3)/(1)	(a)	1.9/2.4	1.56/1.68	1
0010	ADK	0/1	K	-/0	(2)	(a)	1.9/2.4	1.56/1.68	2
0011	SUK	0/1	K	-/0	(2)	(a)	1.9/2.4	1.56/1.68	2
0100	ANK	0/1	K	-/0	(2)	(a)	1.9/2.4	1.56/1.68	3
0101	ORK	0/1	K	-/0	(2)	(a)	1.9/2.4	1.56/1.68	3
0110	XRK	0/1	K	-/0	(2)	(a)	1.9/2.4	1.56/1.68	4
0111	MLK	1	K	0	(1)	(a)	(n+1).1.2	(n+1).0.84	4
0001	AB	0/1	K	-/0	(3)	(c)	1.9/2.4	1.56/1.68	5
1110	CF	1	K	1	(3)	(a) (d)	6.24	4.80	5
1101	CWK	1	K	0	(4)	(a)	2.4	1.68	6
1101	CCK	1	K	1	(4)	(a)	2.4	1.68	6
1100	LCK	1	K	0	(3)	(a)	2.4	1.68	6

Op. Code	Mnemonic	Format	Type	L/S bit	Cond. Reg.	Remarks	Execution time μsec P855	P860	Page
1000	MUK	1	K	0	(2)	(c)	8.52	7.80	7
1001	DVK	1	K	0	(2)	(c)	9.96	9.24	7
1010	DAK	1	K	0	(2)	(c)	4.3	3.24	7
1011	DSK	1	K	0	(2)	(c)	4.3	3.24	7
0111	SLA	0	S	-	(2)	(c) (i)			1
0111	SLA1	0	S	-	(2)	(c) (i)			1
0111	SRA	0	S	-	(1)	(c) (i)			2
0111	SRA1	0	S	-	(1)	(c) (i)			2
0111	SLL	0	S	-	(1)	(c) (i)			2
0111	SLL1	0	S	-	(1)	(c) (i)			2
0111	SRL	0	S	-	(1)	(c) (i)			3
0111	SLC	0	S	-	(1)	(c) (i)			3
0111	SRC	0	S	-	(1)	(c) (i)	**P555**		3
0111	SRC1	0	S	-	(1)	(c) (i)	**n**×0.36+2.28		3
0111	SLN	0	S	n.s.	(3)	(c) (i)			4
0111	SRN	0	S	n.s.	(3)	(c) (i)	**P860**		4
0111	DLA	0	S	-	(2)	(c)	n×0.36+1.92		5
0111	DRA	0	S	-	(1)	(c)			5
0111	DLL	0	S	-	(1)	(c)			6
0111	DRL	0	S	-	(1)	(c)			6
0111	DLC	0	S	-	(1)	(c)			6
0111	DRC	0	S	-	(1)	(c)			7
0111	DLN	0	S	n.s.	(3)	(c)			7
0111	DRN	0	S	n.s.	(3)	(c)			8
1000	CIO	o	I/O	-	(5)	(k)	3.6	2.52	1
1001	INR	0	I/O	-	(5)	(k)	3.6	2.52	1
1001	SST	0	I/O	-	(5)	(k) (l)	3.6	2.52	2
1000	OTR	0	I/O	-	(5)	(k)	3.6	2.52	2
1001	TST	0	I/O	-	(5)	(k)	3.6	2.52	3
1000	WMP	0	I/O	-	(3)	(k)	2.6	2.28	3
1001	RIL	0	I/O	-	(3)	(k)	2.6	2.28	3